WHAT IS CLAIMED IS:

1. A method of forming an anti-fuse on a first semiconductor material of a first conductivity type, the method comprising the steps of:

forming a well in the first semiconductor material, the well having a surface and a second conductivity type;

forming a layer of insulation material on the surface of the well;

removing a first portion of the layer of insulation material to expose a first region on the surface of the well, and a second portion of the layer of insulation material to expose a second region on the surface of the well;

forming a layer of second semiconductor material on the layer of insulation material, the first region, and the second region;

etching the layer of second semiconductor material to form a first section and a second section; and

removing the layer of insulation material between the first and second sections to expose a third region on the surface of the well.

2. The method of claim 1 and further comprising the step of doping the third region with a dopant to form a doped region in the well.

3. The method of claim 1 and further comprising the step of doping the first section and the third region with a dopant of the second conductivity type to dope the first section and form a doped region in the well, the doped region having a dopant concentration greater than a dopant concentration of the well.

4. The method of claim 3 and further comprising the step of doping the second section with a dopant of the first conductivity type to dope the second section.

5. The method of claim 4 and further comprising the step of forming a first layer of silicide on the first section, a second layer of silicide on the second section, and a third layer of silicide on the doped region.

6. The method of claim 5 and further comprising the steps of:

forming a first layer of dielectric material on the first layer of silicide, the second layer of silicide, and the third layer of silicide, the first layer of dielectric material having a top surface; and

forming first contacts through the first layer of dielectric material to make electrical connections with the first layer of silicide, and second contacts through the first layer of dielectric material to make electrical connections with the second layer of silicide.

7. The method of claim 6 wherein the step of forming first and second contacts includes the steps of:

forming first openings in the first layer of dielectric material to expose regions of the first layer of silicide, and second openings in the first layer of dielectric material to expose regions of the second layer of silicide;

depositing a layer of tungsten on the first layer of dielectric material to fill up the first openings and the second openings; and

removing the layer of tungsten from the top surface of the first layer of dielectric material.

8. The method of claim 6 and further comprising the step of forming a first metal trace on the first layer of dielectric material to make electrical connections with the first contacts, and a second metal trace on the first layer of dielectric material to make electrical connections with the second contacts.

9. The method of claim 1 and further comprising the step of forming a first layer of silicide on the first section, a second layer of silicide on the second section, and a third layer of silicide on the third region.

10. The method of claim 9 and further comprising the steps of:

forming a first layer of dielectric material on the first layer of silicide, the second layer of silicide, and the third layer of silicide, the first layer of dielectric material having a top surface; and

forming first contacts through the first layer of dielectric material to make an electrical connection with the first layer of silicide, and second contacts through the first layer of dielectric material to make an electrical connection with the second layer of silicide.

11. The method of claim 10 and further comprising the step of forming a first metal trace on the first layer of dielectric material to make electrical connections with the first contacts, and a second metal trace on the first layer of dielectric material to make electrical connections with the second contacts.

12. The method of claim 3 and further comprising the step of forming a side wall spacer that adjoins the first section over the third

region, and a side wall spacer that adjoins the second section over the third region.

13. The method of claim 9 and further comprising the step of forming a side wall spacer that adjoins the first section over the third region, and a side wall spacer that adjoins the second section over the third region.

14. The method of claim 1 and further comprising the steps of:

forming a first layer of dielectric material over the first section and the second section, and on the third region; and

forming first contacts through the first layer of dielectric material to be electrically connected with the first section, and second contacts through the first layer of dielectric material to be electrically connected with the second section.

15. The method of claim 14 wherein the first and second contacts include tungsten and are free of aluminum.

16. An anti-fuse formed on a first semiconductor material of a first conductivity type, the anti-fuse comprising:

a well formed in the first semiconductor material, the well having a surface, a second conductivity type, and a dopant concentration;

a first doped region of the second conductivity type formed in the well, the first doped region having a dopant concentration that is greater than the dopant concentration of the well;

a second doped region of the first conductivity type formed in the well, the second doped region being spaced apart from the first doped region;

a third doped region formed in the well, the third doped region being spaced apart from the first and second doped regions;

a layer of insulation material formed on the surface of the well, the layer of insulation material having a first opening that exposes the first doped region of the well, a second opening that exposes the second doped region of the well, and a third opening that exposes the third doped region of the well;

a first section of a second semiconductor material formed on the layer of insulation material and the first region;

a second section of the second semiconductor material formed on the layer of insulation material and the second region, the second section being spaced apart from the first section; and

a first layer of dielectric material formed on the first section, the second section, and the third doped region.

17. The anti-fuse of claim 16 wherein the first section includes:

a first polysilicon region; and

a first layer of silicide formed on the first polysilicon region.

18. The anti-fuse of claim 17 wherein the second section includes:

a second polysilicon region; and

a second layer of silicide formed on the second polysilicon region.

19. The anti-fuse of claim 18 and further comprising a third layer of silicide formed on the third doped region.

20. The anti-fuse of claim 19 and further comprising a side wall spacer formed to adjoin the first section over the third doped region.